Amendment of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-3 (cancelled)

4. (currently amended) An integrated circuit computer system on a single integrated circuit comprising:

a processor interconnected with memory and peripheral circuits on said integrated circuit;

a scan-path interface circuit for reading out contents of a predetermined memory or register in said system;

a switching circuit coupled to said processor and to said scan-path interface circuit for switching said scan-path interface circuit between a first mode in which it is enabled and a second mode in which it is disabled; and

a security mechanism comprising:

a plurality of input ports for said processor;

a program stored in said memory to operate said processor to receive a plurality of commands applied to said plurality of input ports and to process said commands to produce a password which is compared with a predetermined password;

and wherein said switching circuit is responsive to said comparison.

5. (previously presented) The computer system of claim 4 wherein said program operates said processor to receive said plurality of commands which are applied to said plurality of ports in a specific time sequence.

6. (previously presented) The computer system of claim 4 further comprising a pair of registers, one of said registers receiving said produced password and the other of said registers containing said predetermined password; and a comparator for comparing the contents of said registers for controlling said switching circuit.

7. (previously presented) The computer system of claim 5 further comprising a pair of registers, one of said registers receiving said produced password and the other of said registers containing said predetermined password; and a comparator for comparing the contents of said registers for controlling said switching circuit.

8. (currently amended) In an integrated circuit computer system on a single integrated circuit having a processor interconnected with memory and peripheral circuits on said integrated circuit, a security system comprising:

a plurality of input ports for said processor;

a program stored in said memory and operable to control said processor to receive a plurality of commands applied to said plurality of input ports and operable to control said processor to process said commands to produce a password which is compared with a predetermined password.

9. (previously presented) The security system of claim 8 further comprising a switching circuit coupled to a scan-path interface circuit and being responsive to said comparison for switching said scan-path interface circuit between a first mode in which it is enabled and a second mode in which it is disabled.

10. (previously presented) The security system of claim 8 wherein said program operates said processor to receive said plurality of commands which are applied to said plurality of ports in a specific time sequence.

11. (previously presented) The security system of claim 8 further comprising a pair of registers, one of said registers receiving said produced password and the other of

said registers containing said predetermined password; and a comparator for comparing the contents of said registers for controlling a switching circuit.

12. (previously presented) The security system of claim 9 further comprising a pair of registers, one of said registers receiving said produced password and the other of said registers containing said predetermined password; and a comparator for comparing the contents of said registers for controlling said switching circuit.

13. (previously presented) The security system of claim 10 further comprising a pair of registers, one of said registers receiving said produced password and the other of said registers containing said predetermined password; and a comparator for comparing the contents of said registers for controlling a switching circuit.

14. (currently amended) A security system for [[an]] a single chip integrated circuit computer system comprising:

means on said chip for applying a plurality of commands to a plurality of ports for [[a]] an on-chip processor of said system;

a program stored in a memory on said chip coupled to said processor and operable to control said processor to process said plurality of commands to produce a password;

means on said chip for comparing said produced password with a predetermined password.

15. (previously presented) The security system of claim 14 wherein said program is operable to control said processor to receive said plurality of commands which are applied to said plurality of ports in a specific time sequence.

16. (previously presented) The security system of claim 14 further comprising a pair of registers, one of said registers receiving said produced password and the other of said registers containing said predetermined password; and a comparator for comparing the contents of said registers and generating a comparison signal.

17. (previously presented) The security system of claim 15 further comprising a pair of registers, one of said registers receiving said produced password and the other of said registers containing said predetermined password; and a comparator for comparing the contents of said registers and generating a comparison signal.

18. (previously presented) The security system of claim 14 further comprising a scan-path interface circuit for reading out contents of a predetermined memory or register in said system and a switching circuit responsive to said comparison to switch operation of said scan-path interface circuit between enabled and disabled modes.

19. (previously presented) The security system of claim 15 further comprising a scan-path interface circuit for reading out contents of a predetermined memory or register in said system and a switching circuit responsive to said comparison to switch operation of said scan-path interface circuit between enabled and a disable modes.

20. (previously presented) The security system of claim 16 further comprising a scan-path interface circuit for reading out contents of a predetermined memory or register in said system and a switching circuit responsive to said comparison to switch operation of said scan-path interface circuit between enabled and a disable modes.

21. (previously presented) The security system of claim 17 further comprising a scan-path interface circuit for reading out contents of a predetermined memory or register in said system and a switching circuit responsive to said comparison to switch operation of said scan-path interface circuit between enabled and a disable modes.